|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| InstName | Opcode | jump | branch | memRead | memToReg | memWrite | aluSrc | RegWrite | RegDst |
| add | 100000 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| sub | 100010 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| mult | 011000 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| and | 100100 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| or | 100101 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| addi | 001000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| sll | 000000 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| slt | 101010 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| mfhi | 010000 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| mflo | 010010 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| lw | 100011 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| sw | 101011 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| beq | 000100 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| bleq | 000110 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| j | 000010 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| myIns | 111111 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |

In our design of control unit, we did not include AluOp control signal because our Alu control, inside ALU, is taking opcode of the instruction as input directly and deciding which Alu operation will be done. Other control signals are one bit and working the same as MIPS. However, in R type instructions, both aluSrc and regDst control signals which we directed to multiplexers are 1. In I type instructions aluSrc and regDst are 0.